IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Masaharu Nagai et al.	Art Unit	: Unknown
Serial No.	: New Application	Examiner	: Unknown
Filed	: October 29, 2003		
Title	: METHOD FOR REMOVING RESIST PATTERN AND METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Applicants submit the references listed on the attached form PTO-1449.

This statement is being filed with the application. Accordingly, only copies of foreign patent documents and non-patent literature are enclosed. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: October 29, 2003

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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 12732-171001	Application No. New Application
Information Disclosure Stat ment by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Masaharu Nagai et al.	
		Filing Date October 29, 2003	Group Art Unit Unknown

U.S. Patent Documents

Examiner Initial	Desig. ID	Application Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	10/405,908	Pending	Masaharu Nagai et al.			04/03/2003
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	AL	2002-033273	01/31/2002	JAPAN			ABS	
	AM							
	AN							
	AO							
	AP							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	AQ	
	AR	
	AS	
	AT	

Examiner Signature	Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

DIALOG(R)File 352:Derwent WPI

014555308 **Image available**
WPI Acc No: 2002-376011/200241
XRAM Acc No: C02-106455
XRPX Acc No: N02-293951
Preparation method for semiconductor device, involves forming resist pattern on film followed by pre-baking, exposure, baking, developing, post-baking at preset temperature and dry etching
Patent Assignee: SEMICONDUCTOR ENERGY LAB (SEME)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2002033273	A	20020131	JP 2001144021	A	20010514	200241	B

Priority Applications (No Type Date): JP 2000140319 A 20000512
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2002033273	A		20	H01L-021/027	

Abstract (Basic): JP 2002033273 A

NOVELTY - A resist pattern (106) is formed on a film followed by pre-baking, exposure, baking after exposure, developing and post-baking. The baking temperature after exposure is the same as that of post-baking temperature or more. Subsequently dry etching of the film is carried out to obtain the semiconductor device.

USE - For formation of semiconductor device having circuit and thin film transistor (TFT) structure, used in active matrix type liquid crystal display technique.

ADVANTAGE - The preparation of semiconductor device reduces the volumetric shrinkage phenomena by desolvent during post-baking. The resist pattern has a highly precise controlled taper angle which inhibits a fluctuation of the gate electrode. The manufacturing method forms the dimension of LDD region efficiently. The manufacturing method provides stable etching form depending on pattern size. The quality of a semiconductor device and yield are thus improved. The substrate surface fluctuation and TFT characteristics variation is reduced.

DESCRIPTION OF DRAWING(S) - The figure shows the substrate sectional drawing of the preparation process of the GOLD structure TFT. (Drawing includes non-English language text).

Resist pattern (106)

pp; 20 DwgNo 4/13

Title Terms: PREPARATION; METHOD; SEMICONDUCTOR; DEVICE; FORMING; RESIST; PATTERN; FILM; FOLLOW; PRE; BAKE; EXPOSE; BAKE; DEVELOP; POST; BAKE; PRESET; TEMPERATURE; DRY; ETCH
Derwent Class: L03; P84; U11; U12
International Patent Class (Main): H01L-021/027
International Patent Class (Additional): G03F-007/38; G03F-007/40; H01L-021/28; H01L-021/336; H01L-029/786
File Segment: CPI; EPI; EngPI

07164889

MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

PUB. NO.: **2002-033273** [JP 2002033273 A]
PUBLISHED: January 31, 2002 (20020131)
INVENTOR(s): UEHARA ICHIRO
SUZAWA HIDEOMI
ONO KOJI
APPLICANT(s): SEMICONDUCTOR ENERGY LAB CO LTD
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FILED: May 14, 2001 (20010514)
PRIORITY: 2000-140319 [JP 2000140319], JP (Japan), May 12, 2000 (20000512)
INTL CLASS: H01L-021/027; G03F-007/38; G03F-007/40; H01L-021/28; H01L-021/336; H01L-029/786

ABSTRACT

PROBLEM TO BE SOLVED: To solve the problem of dependency of a resist pattern side-wall taper angle on an area, in a photolithography utilizing diazonaphthoquinone(DNQ)-novolak resin positive resist in a gate electrode forming process for a TFT.

SOLUTION: In order to suppress fluctuation in taper angle due to variation in scale of resist pattern, a volume contraction phenomenon due to deliquoring at post baking where only the resist pattern is baked is reduced, regardless of presence of PEB process. For that purpose, the deliquoring of remaining solvent inside a resist film is preferred to be promoted in a stage before patterning in a development process, in short, a stage of the resist film. Specifically, a baking condition is limited so that a PEB temperature is equal to or above a postbaking temperature for including the PEB process while the baking condition is so limited that the pre-baking temperature is ±10°C of the post baking temperature with no PEB process.